

Ask the Applications Engineer—5

High-Speed Comparators Provide Many Useful Circuit Functions When Used Correctly

by John Sylvan

Question: Why can't I just use a standard op amp in a high-gain or open-loop configuration as a voltage comparator?

You can—if you are willing to accept response times in the tens of microseconds. Indeed, if in addition you require low bias-currents, high-precision and low offset voltages, then an op amp might be a better choice than most standard voltage comparators. But since most op amps have internal phase/frequency compensation for stability with feedback, it's difficult to get them to respond in nanoseconds. On the other hand, a low-cost popular comparator, the LM311, has a response time of 200 ns.

Also the output of an operational amplifier is not readily matched to standard logic levels. Without external clamping or level-shifting, an op amp operating as a comparator will swing to within a few volts of the positive and negative supplies, which is incompatible with standard TTL or CMOS logic levels.

My comparator oscillates uncontrollably. Why does this happen?

Examine the power-supply bypassing. Even a few inches of PC trace on the supply lines can add unacceptable dc resistance and inductance. As a result, transient currents while the output is switching may cause supply-voltage fluctuations, which are fed back to the input through the ground and supply lines. Install low-loss capacitors (0.1 μ F ceramic capacitors) as close as possible to the supply pins of the comparator to serve as a low-impedance reservoir of energy during high-speed switching.¹

I've installed bypass capacitors, but I still can't keep my high-speed comparator from oscillating. Now what's the problem?

It could be the comparator's ground connection. Make sure that the ground lead is as short as possible and connected to a low-impedance ground point to minimize coupling through lead inductance. Use a ground plane if possible and avoid sockets.

Another cause of the oscillation may be a high source impedance and stray capacitance to the input. Even a few thousand ohms of source impedance and picofarads of stray capacitance can cause unruly oscillations. Keep leads short, including the ground clip of your scope probe. For best measurement results use the shortest possible ground lead to minimize its inductance (<1").

With a slowly moving input signal, my comparator seems to "chatter" as it passes through the transition voltage. Why can't I obtain a single clean transition from the device?

A comparator's high gain and wide bandwidth are typically the source of this problem. Any noise is amplified, and as the signal passes through the transition region, the noise can cause a fast-responding amplifier's output to bounce back and forth. Also, since the device's sensitivity (i.e., gain) is higher during a transition, the tendency to oscillate due to feedback increases. If possible, filter the signal to minimize noise accompanying it.

¹A useful discussion of comparator foibles can be found in *Troubleshooting Techniques Quash Spurious Oscillations*, by Bob Pease, *EDN*, September 14, 1989, pp. 152-6

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Then try using hysteresis which, like backlash in gear trains, requires the input to change by a certain amount before a reversal occurs. For example, after a high-to-low transition on the AD790, its built-in hysteresis requires the input voltage (positive input) to increase by 500 μ V to produce a low-to-high transition.

If my comparator does not have internal hysteresis, can I add it externally?

Yes, with external positive feedback. This is done by feeding a small fraction of the output of the comparator back to the positive input. This simple technique is shown in Figure 1. The hysteresis voltage from the lower transition point to the upper transition point will depend on the value of the feedback resistor, R_F , the source resistance, R_S , low output level, V_{low} , and high output level, V_{high} . The low and high transition points are set by:

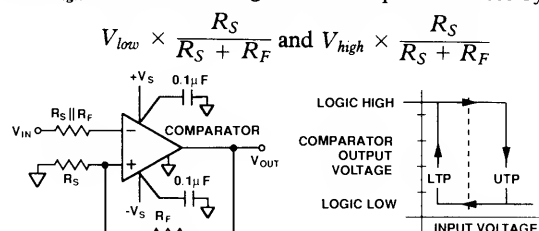
$$V_{low} \times \frac{R_S}{R_S + R_F} \text{ and } V_{high} \times \frac{R_S}{R_S + R_F}$$


Figure 1. Applying external hysteresis to a comparator.

Figure 2 shows how adding external hysteresis can "clean up" a comparator's response. Figure 2a shows the response of a comparator with bipolar output swing without hysteresis. As the triangular-wave input (trace A) passes through the transition point (ground), the device oscillates vigorously (and couples a portion of the oscillation into ground and the signal-source). Figure 2b depicts the response of the same comparator with 5 mV of external hysteresis applied; it shows a much cleaner transition.

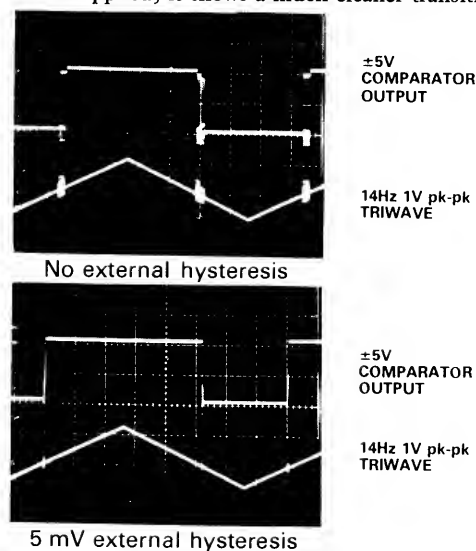


Figure 2. Hysteresis helps clean up comparator response.

A problem encountered with external hysteresis is that output voltage depends on supply voltage and loading. This means the hysteresis voltage can vary from application to application; though this affects resolution, it need not be a serious problem, since the hysteresis is usually a very small fraction of the range and can tolerate a safety margin of two or three (or more) times what one might calculate. Swapping in a few comparators can help confidence in the safety margin. Don't use wirewound resistors for feedback; their inductance can make matters worse.

What's the difference between propagation delay and prop-delay dispersion? Which of the two specifications is of most concern?

Propagation delay is the time from when the input signal crosses the transition point to when the output of the comparator actually switches. Propagation-delay dispersion is the variation in prop delay as a function of overdrive level. If you're using a comparator in pin-drive electronics in an automatic test system, then prop-delay dispersion will determine the maximum edge resolution. In contrast, propagation delay can be considered as a fixed time offset and therefore compensated for by other techniques.

I have a +5-volt system and don't want to add an additional supply voltage; can I use my comparator with a single supply?

Yes, but to establish the threshold use an adequately bypassed stable reference source well within the common-mode range of the device. The signal level is also to be referenced to this source.

I sometimes see unexpected behavior in my comparator. What could be the cause of this problem?

Examine the common-mode range of the input signal. Unlike operational amplifiers, that usually operate with the input voltages at the same level, comparators typically see a large differential voltage swings at their inputs. If the inputs exceed the device's specified common-mode range (even though within the specified signal range), the comparator may respond erroneously. For proper operation, ensure that *both* input signals do not exceed the common-mode range of the specific comparator. For example, the AD790 has a $\pm V_S$ differential input range, but its common-mode range is from $-V_S$ to 2 volts below $+V_S$.

Can you suggest a circuit that performs autozeroing when the comparator is off-line to minimize drift?

Try the circuit shown in Figures 3 and 4. In the Calibrate mode, the input is disconnected and the positive input of the comparator is switched to ground. The comparator is connected in a loop with a pair of low-voltage sources of opposing polarity charging a buffered capacitor in response to the comparator's output state.

If the comparator's minus input terminal is above ground, then the comparator output will be low, the 1- μ F capacitor will be connected to the negative voltage (-365 mV) and the voltage from the buffer amplifier will ramp down until it is below the plus input (ground)—plus hysteresis and any offsets—at which point the comparator switches. If it is below ground, the comparator's output will be high, the capacitor will be connected to the positive voltage ($+365$ mV), the output from the buffer amplifier ramps up. In the final state, each time the comparator switches (when the ramped change exceeds the hysteresis voltage), the polarity of the current is reversed; thus the capacitor voltage averages out the offsets of the buffer and comparator.

At the end of the Calibrate cycle, the JFET switch is opened, with the capacitor charged to a voltage equal to the offsets of the comparator and buffer \pm the hysteresis voltage. At the same time, the Calibrate signal goes low, disabling the feedback to the polarity switch and connecting the input signal to the comparator.

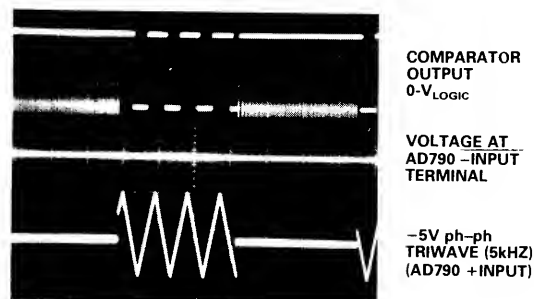


Figure 4. Comparator output, buffer output, and comparator input.

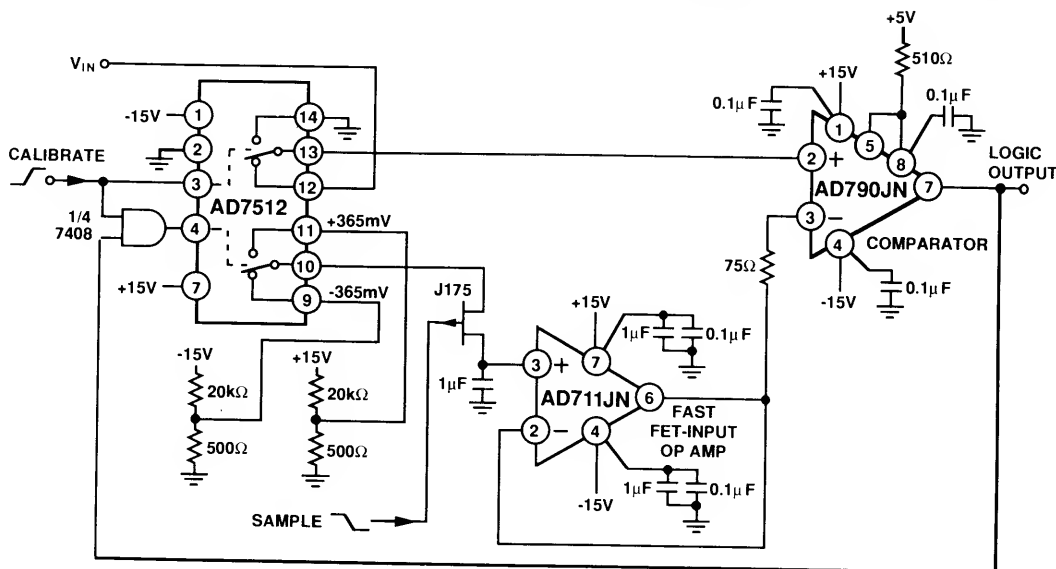


Figure 3. Autozeroed comparator integrates out offsets during calibration cycle.